GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

Course File

Subject: Analog and Digital Electronic Lab

Subject Code: GR17A2046

Academic Year: 2018-19

Regulation: GR17

Year: II **Semester:** II

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

Vision of the Institute

To be among the best of the institutions for engineers and technologists with attitudes, skills and knowledge and to become an epicenter of creative solutions.

Mission of the Institute

To achieve and impart quality education with an emphasis on practical skills and social relevance.

Vision of the Department

To impart technical knowledge and skills required to succeed in life, career and help society to achieve self sufficiency.

Mission of the Department

- To become an internationally leading department for higher learning.
- To build upon the culture and values of universal science and contemporary education.
- To be a center of research and education generating knowledge and technologies which lay groundwork in shaping the future in the fields of electrical and electronics engineering.
- To develop partnership with industrial, R&D and government agencies and actively participate in conferences, technical and community activities.

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

Programme Educational Objectives (B.Tech. – EEE)

This programme is meant to prepare our students to professionally thrive and to lead.
During their progression:

Graduates will be able to

PEO 1: Have a successful technical or professional careers, including supportive and leadership roles on multidisciplinary teams.
PEO 2: Acquire, use and develop skills as required for effective professional practices.
PEO 3: Able to attain holistic education that is an essential prerequisite for being a responsible member of society.
PEO 4: Engage in life-long learning, to remain abreast in their profession and be leaders in our technologically vibrant society.

Programme Outcomes (B.Tech. – EEE)

At the end of the Programme, a graduate will have the ability to

PO 1: Apply knowledge of mathematics, science, and engineering.
PO 2: Design and conduct experiments, as well as to analyze and interpret data.
PO 3: Design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
PO 4: Function on multi-disciplinary teams.
PO 5: Identify, formulates, and solves engineering problems.
PO 6: Understanding of professional and ethical responsibility.
PO 7: Communicate effectively.
PO 8: Broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context.
PO 9: Recognition of the need for, and an ability to engage in life-long learning.
PO 10: Knowledge of contemporary issues.
PO 11: Utilize experimental, statistical and computational methods and tools necessary for engineering practice.
PO 12: Demonstrate an ability to design electrical and electronic circuits, power electronics, power systems; electrical machines analyze and interpret data and also an ability to design digital and analog systems and programming them.

PEOs & POs Mapping

Programme Educational Objectives (PEOs)	Programme Outcomes (POs)											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
1	M	M	-	-	H	-	-	H	H	-	H	H
2	-	-	M	M	H	H	H	-	-	-	-	H
3	-	-	-	-	H	H	M	M	M	M	H	H
4	-	-	-	M	M	H	M	H	H	-	M	H

* H: Strongly Correlating (3); M: Moderately Correlating (2)& L: Weakly Correlating (1)

HOD-EEE

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

GRIET/DAA/1H/G/18-19 05 May 2018

ACADEMIC CALENDAR
Academic Year 2018-19

II B.TECH – FIRST SEMESTER

S. No.	EVENT	PERIOD	DURATION
1	1st Spell of Instructions	02-07-2018 to 05-09-2018	9 Weeks3 Days
2	1st Mid-term Examinations	06-09-2018 to 08-09-2018	3 Days
3	2nd Spell of Instructions	10-09-2018 to 27-10-2018	7 Weeks
4	2nd Mid-term Examinations	29-10-2018 to 31-10-2018	3 Days
5	Preparation	01-11-2018 to 07-11-2018	1Week
6	**End Semester Examinations (Theory/ Practicals) Regular/Supplementary**	**08-11-2018 to 08-12-2018**	**4 Weeks 3 Days**
7	Commencement of Second Semester, A.Y 2018-19	10-12-2018	

IIB.TECH – SECOND SEMESTER

S. No.	EVENT	PERIOD	DURATION
1	1st Spell of Instruction	10-12-2018 to 06-02-2019	8 Weeks3 days
2	1st Mid-term Examinations	07-02-2019 to 09-02-2019	3 Days
3	2nd Spell of Instruction	11-02-2019 to 03-04-2019	**7 Weeks 3 Days**
4	2nd Mid-term Examinations	04-04-2019to 06-04-2019	3 Days
5	Preparation	08-04-2019 to 17-04-2019	**1 Week 3 Days**
6	**End Semester Examinations(Theory/ Practicals) Regular**	18-04-2019 to 08-05-2019	3 Weeks
7	**Supplementary and Summer Vacation**	**09-05-2019 to 22-06-2019**	**6 Weeks 3 Days**
8	Commencement of First Semester, A.Y 2019-20	24-06-2019	

Copy to Director, Principal, Vice Principal, DOA, DOE, Balaji Kumar, DCGC, All HODs

(Dr. K. Anuradha)
Dean of Academic Affairs

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

Gokaraju Rangaraju Institute of Engineering and Technology				
Department of Electrical and Electronics Engineering				
2018-19 II sem Subject Allocation sheet				
	GRIET/EEE/05B/G/18-19		**30.10.18**	
	II YEAR(GR17)	Section-A	Section-B	
	Managerial Economics and Financial Analysis			
	Power Generation and Distrubution	SN	SN	
	AC Machines	VVSM	VVSM	
	Control Systems	Dr DGP	MS	
	Princeples of Digital Electronics	PRK	PRK	
	AC Machines Lab	PPK/DSR	PPK/DSR	
	Control Systems Lab	MS/PSVD	MS/PSVD	
	Analog and Digital Electronics Lab	**RAK/DKK**	**RAK/DKK**	
	Value Education and Ethics			
	Gender Sensitization Lab	MS/PSVD	MS/PSVD	
	III YEAR (GR15)			
	Computer Methods in Power systems	VVRR/MP	VVRR/MP	
	Switch Gear & Protection	PSVD	Dr JSD	
	Management Science			
	Utilization of Electrical Energy	MRE	MRE	
	Non Conventional Sources of Energy			
	Neural and Fuzzy Systems			
	Sensors&Transducers	UVL	UVL	
	Power Systems Lab	GSR/YSV	GSR/YSV	
	Advanced English Communications Skills Lab			
	Industry Oriented Mini Project Lab	PPK/AVK/Dr JP	MP/Dr JP	
	IV YEAR (GR15)			
	Programmable Logic Controllers	PK		
	Flexible AC Transmission Systems	Dr TSK		
	EHV AC Transmission			
	Power System Automation			
	Modern Power Electronics	AVK		
	DSP Based Electromechanical Systems			
	Advaced Control Systems			

Department of Electrical & Electronics Engineering

	Programmable Logic Controllers-Lab	VVSM	PK	
	Main Projects	RAK/Dr SVJK	PK/VVRR	
	M.Tech PE			
	Modeling and Analysis of Electrical Machines	Dr BPB		
	Digital control of power Electronics and Drive Systems	Dr DGP		
	FACTS and Custom power Devices	Dr TSK		
	Smart Grids	VVRR		
	Audit Course -2	YSV/UVL		
	Power Quality Lab	Dr BPB		
	Digital Signal Processing Lab	AVK		
	MINI Projects	Dr JP/GSR		
	M.Tech PS			
	Digital Protection of Power System	Dr JSD		
	Power System Dynamics -II	Dr SVJK		
	FACTS and Custom power Devices	Dr TSK		
	Smart Grids	VVRR		
	Audit Course -2	YSV/UVL		
	Power Quality Lab	Dr BPB		
	Power System Protection Lab	VUR		
	MINI Projects	Dr JP/GSR		
	Other Dept.			
	BEE (I YEAR) CSE (6)	MNSR,MK,MVK,		
	BEE Lab	MNSR,MK,MVK,YSV,VUR,PS,UVL,MRE,GBR		
	EET (II YEAR) Mech (2)	KS	KS	
	EET LAB (II TEAR) Mech (2)	KS,DKK,PPK,		

HoD-EEE

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Department of Electrical & Electronics Engineering

GRIET/PRIN/06/G/01/18-19 wef: 10 Dec 2018

B.Tech - EEE – A II Year - II Semester

Day/Hour	9:00 - 9:50	9:50 - 10:40	10:40 - 11:30	11:30-12:00	12:00-12:45	12:45 - 1:30	1:30 - 2:15	2:15 - 3:00
MONDAY	MEFA		PGD	BREAK	CS		PDE	
TUESDAY	MEFA		ACM		PGD		CS	
WEDNESDAY	VEE		PDE		PGD		ACM	
THURSDAY	CS		ACM		**CS/GS LAB(A1) /ADE Lab(A2)**			
FRIDAY	ACM		PDE		CS/GS LAB(A2) /ACM Lab(A1)			
SATURDAY	PDE		PGD		**ACM Lab(A2) / ADE Lab (A1)**			

Room No.	
Theory	4401
Lab	**2106-07/4505/4507**
Class Incharge:	V V S Madhuri

Subject Code	Subject Name	Faculty Code	Faculty Name	Almanac	
MEFA	Managerial Economics and Financial Analysis	KL	K Latha	1st Spell of Instructions	10-12-2018 to 06-02-2019
PGD	Power Generation and Distrubution	SN	Syed Sarfaraz Nawaz	1st Mid-term Examinations	07-02-2019 to 09-02-2019
ACM	AC Machines	VVSM	VVS Madhuri	2nd Spell of Instructions	11-02-2019 to 03-04-2019
CS	Control Systems	Dr DGP	Dr D G Padhan	2nd Mid-term Examinations	04-04-2019 to 06-04-2019
PDE	Principles of Digital Electronics	PRK	P Ravi Kanth	Preparation	08-04-2019 to 17-04-2019
ACM Lab	AC Machines Lab	PPK/DSR	P Praveen Kumar/ D Srinivasa Rao	End Semester Examinations (Theory/ Practicals) Regular	18-04-2019 to 08-05-2019
CS Lab	Control Systems Lab	MS/PSVD	M Srikanth /P Srividya Devi		
ADE Lab	**Analog and Digital Electronics Lab**	**RAK/DKK**	**R Anil Kumar/D Karuna Kumar**	Supplementary and Summer Vacation	09-05-2019-to 22-06-2019
VEE	Value Education and Ethics	KL	K Latha		
GS Lab	Gender Sensitization Lab	MS/PSVD	M Srikanth /P Srividya Devi	Commencement of Second Semester , AY	24-06-2019

HOD **Co-ordinator** **DAA**

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

GRIET/PRIN/06/G/01/18-19 wef: 10 Dec 2018

B.Tech - EEE - B II Year - II Semester

Day/Hour	9:00 - 9:50	9:50 - 10:40	10:40 - 11:30	11:30-12:00	12:00-12:45	12:45 - 1:30	1:30 - 2:15	2:15 - 3:00
MONDAY	CS		PDE	BREAK	**CS/GS LAB(B1) /ADE Lab(B2)**			
TUESDAY	CS		PDE		CS/GS LAB(B2) /ACM Lab (B1)			
WEDNESDAY	PGD		ACM		**ACM Lab(B2) / ADE Lab(B1)**			
THURSDAY	MEFA		CS		PGD		ACM	
FRIDAY	MEFA		CS		ACM		PDE	
SATURDAY	VEE		ACM		PDE		PGD	

Room No.	
Theory	4402
Lab	**2106-07/4505/4507**
Class Incharge:	V V S Madhuri

Subject Code	Subject Name	Faculty Code	Faculty Name	Almanac	
MEFA	Managerial Economics and Financial Analysis	KL	K Latha	1st Spell of Instructions	10-12-2018 to 06-02-2019
PGD	Power Generation and Distrubution	SN	Syed Sarfaraz Nawaz	1st Mid-term Examinations	07-02-2019 to 09-02-2019
ACM	AC Machines	VVSM	VVS Madhuri	2nd Spell of Instructions	11-02-2019 to 03-04-2019
CS	Control Systems	MS	M Srikanth	2nd Mid-term Examinations	04-04-2019 to 06-04-2019
PDE	Principles of Digital Electronics	PRK	P Ravi Kanth	Preparation	08-04-2019 to 17-04-2019
ACM Lab	AC Machines Lab	PPK/DSR	P Praveen Kumar/ D Srinivasa Rao	End Semester Examinations (Theory/ Practicals) Regular	18-04-2019 to 08-05-2019
CS Lab	Control Systems Lab	MS/PSVD	M Srikanth /P Srividya Devi		
ADE Lab	**Analog and Digital Electronics Lab**	**RAK/DKK**	**R Anil Kumar/D Karuna Kumar**	Supplementary and Summer Vacation	09-05-2019-to 22-06-2019
VEE	Value Education and Ethics	KL	K Latha		
GS Lab	Gender Sensitization Lab	MS/PSVD	M Srikanth /P Srividya Devi	Commencement of Second Semester , AY	24-06-2019

HOD **Co-ordinator** **DAA**

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

Syllabus - Analog & Digital Electronics Lab
Course Code: GR17A2046
B.Tech II Year II Sem

Contents:

1. Design of Operational Amplifier as proportional Amplifier
2. Design of Operational Amplifier as integrator
3. Design of Operational Amplifier as differential amplifier
4. Design of Operational Amplifier as summation amplifier
5. Design of Operational Amplifier for multiplying two time varying signals
6. Design of Operational Amplifier for generation of triangle wave
7. Design of Operational Amplifier for generation of Square
8. Design of Operational Amplifier for generation of sin wave
9. 555 timer as basic application of generating train of pulses
10. 555 timer as speed sensor / frequency to Voltage Converter
11. Design of Operational Amplifier as D/A converter
12. Design of Operational Amplifier as V/f to F/v converter
13. All gates using Xilinx software with Verilog code
14. 7800 series & I C's and their applications
15. Combination circuits
16. Multiplexer and De multiplexer
17. Flip Flops implementation using Xilinx Software
18. Introduction to logic gates using Xilinx in Cool runner CPLD board

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Department of Electrical & Electronics Engineering

Sessional Question Paper & Soft Copy of Notes/Ppt/Slides & Tutorial Sheets With Solution & Lecture Notes

1. A) Execute an amplifier circuit whose output signal is equal to input signal using operational amplifier and Analog Discovery Kit.

   B) Execute the operation of Full Subtractor using Xilinx Software with Verilog Code

2. A) Execute an amplifier circuit whose output signal is two times that of input signal using operational amplifier and Analog Discovery Kit.

   B) Execute the operation of Half Subtractor using Xilinx Software with Verilog Code

3. A) Execute an amplifier circuit whose output signal is two times that of input signal with a phase shift of 180 degrees using operational amplifier and Analog Discovery Kit.

   B) Execute the operation of 2x4 Decoder using Xilinx Software with Verilog Code

4. A) Execute an amplifier circuit which generates a ‘Triangular’ waveform using operational amplifier and Analog Discovery Kit.

   B) Execute the operation of NOR and OR logic gate using Xilinx Software with Verilog Code

5. A) Execute an amplifier circuit which generates a ‘Square’ waveform for a given ‘Triangular’ input signal using operational amplifier and Analog Discovery Kit.

   B) Execute the operation of NAND and AND logic gate using Xilinx Software with Verilog Code

6. A) Execute an amplifier circuit whose output is sum of two input signals using operational amplifier and Analog Discovery Kit.

   B) Execute the operation of 2x1 Multiplexer using Xilinx Software with Verilog Code

7. A) Execute an amplifier circuit whose output is difference of two input signals using operational amplifier and Analog Discovery Kit.

   B) Execute the operation of 2x4 Decoder using Xilinx Software with Verilog Code

8. A) Execute an amplifier circuit which can be used for generating ‘Square’ wave using operational amplifier and Analog Discovery Kit.

B) Execute the operation of Half Adder using Xilinx Software with Verilog Code

9. A) Execute an amplifier circuit which can be used for generating inverted cos waveform for a given sine wave form input signal using operational amplifier and Analog Discovery Kit.

   B) Execute the operation of XOR and XNOR logic gates using Xilinx Software with Verilog Code

10. A) Execute an Astable Multivibrator application using Timer and Analog Discovery Kit.

    B) Execute the working of OR and AND logic gates using Xilinx Software with Verilog Code

11. A) Execute an amplifier which shifts the sine waveform by an angle of 90 degrees using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of NAND and NOR logic gates using Xilinx Software with Verilog Code

12. A) Execute an amplifier circuit which generates a 'Square' waveform for a given 'Triangular' input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of Half Subtractor with Verilog Code using Xilinx Software

13. A) Execute an amplifier circuit which generates a 'Triangular' waveform for a given 'Square' input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of Half Adder with Verilog Code using Xilinx Software

14. A) Execute an amplifier circuit which works as integral of input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of Half Adder with Verilog Code using Xilinx Software

15. A) Execute an amplifier circuit which generates a 'Triangular' waveform for a given 'Square' input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the working of NAND and AND logic gate using Xilinx Software with Verilog Code

16. A) Execute an amplifier circuit which works as a summer/adder of two signals using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of 2x1 Multiplexer using Xilinx Software with Verilog Code

17. A) Execute an amplifier circuit whose output is subtractor of two input signals using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of 2x4 Decoder using Xilinx Software with Verilog Code

18. A) Execute an amplifier circuit which works as a 'Square' wave oscillator using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of Half Adder using Xilinx Software with Verilog Code

19. A) Execute an amplifier circuit which 'Triangular' wave form generator without giving any input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of XOR and XNOR logic gates using Xilinx Software with Verilog Code

20. A) Execute a Timer application which used to generate train of pulses with certain frequency using IC and Analog Discovery Kit.

    B) Execute the operation of half Subtractor using Xilinx Software with Verilog Code

21. A) Execute an amplifier circuit which amplifies the output signal up to the Two times of the given input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of XOR and NAND logic gates using Xilinx Software with Verilog Code

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22. A) Execute an amplifier circuit whose output signal is 1.5 times that of input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of Half Subtractor using Xilinx Software with Verilog Code

23. A) Execute an amplifier circuit whose output signal is 1.5 times that of input signal with a phase shift of 180 degrees using operational amplifier and Analog Discovery Kit.

B) Execute the operation of Full Subtractor using Xilinx Software with Verilog Code

24. A) Execute an amplifier circuit which generates a Triangular waveform for a given 'Square' input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of XOR and XNOR logic gates using Xilinx Software with Verilog Code

25. A) Execute an amplifier circuit which works as differential of input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of NAND and AND logic gate using Xilinx Software with Verilog Code

26. A) Execute a Timer application which used to generate train of pulses with certain frequency using IC and Analog Discovery Kit.

    B) Execute the operation of 2x1 Multiplexer using Xilinx Software with Verilog Code .

22. A) Execute an amplifier circuit which works as a summer/adder of two signals using operational amplifier and Analog Discovery Kit.

    C) Execute the operation of 2x4 Decoder using Xilinx Software with Verilog Code

27. A) Execute an amplifier circuit which generates 'Square' waveform without considering any input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of Half Adder using Xilinx Software with Verilog Code

28. A) Execute an amplifier circuit which generates 'Triangular' waveform without considering any input signal using operational amplifier and Analog Discovery Kit.

    B) Execute the operation of XOR and XNOR logic gates using Xilinx Software with Verilog Code

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

COURSE OBJECTIVES

Academic Year : 2018-2019

Semester : II

Name of the Program: EEE…… B.Tech …II/II…..… Section: A,B

Course/Subject: ADE Lab……Code: …GR17A2046

Name of the Faculty: D.Karunakumar Dept: ……..EEE……
Designation: Assistant professor

On completion of this Subject/Course the student shall be able to:

S.No	Course Objectives
1.	Concept of Operation Amplifier and 555 Timers.
2.	Classification of Analog I C's and Digital I C's
3.	Execution of the oscillators circuits, amplifiers circuits
4.	Concept of different types of waveform generators, clock pulse generation and digital logic implementation
5.	Knowledge on output waveforms and their functionality
6.	Knowledge on amplifiers, waveform generators and simple logic circuits
7.	Knowledge on analog computer and counters

Signature of HOD Signature of faculty

Date: Date:

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INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

COURSE OUTCOMES

Academic Year : 2018-2019

Semester : II

Name of the Program: EEE…… B.Tech …II/II…..… Section: A,B

Course/Subject: ADE Lab…… Code:GR17A2046

Name of the Faculty: D.Karunakumar Dept: ……..EEE……

Designation: Assistant professor

The expected outcomes of the Course/Subject are:

S.No	Course Outcomes
1.	Recall the working operation of Operational Amplifiers, 555 Timer and their applications
2.	Compare the Digital and Analog IC's
3.	Practice the amplifiers, waveform generators and oscillator circuits
4.	Differentiate the integrators and differentiators working operation
5.	Judge the different waveforms and their applications
6.	Predict the circuit output waveform and its value.
7.	Construct the Digital Logic Function and analog circuits.

Signature of HOD Signature of faculty

Date:

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INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

GUIDELINES TO STUDY THE COURSE / SUBJECT

Academic **Y**ear : 2018-2019

Semester : II

Name of the Program: B.Tech Year: II Section: A/B
Course/Subject: ADE Lab Course Code: GR17A2046

Name of the Faculty: D Karunakumar

Designation: ASST.PROFESSOR.

Guidelines to study the Course/ Subject: ADE Lab

CourseDesignandDeliverySystem(CDD):

- The Course syllabus is written into number of learning objectives and outcomes.
- These learning objectives and outcomes will be achieved through lectures, assessments, assignments, experiments in the laboratory, projects, seminars, presentations, etc.
- Every student will be given an assessment plan, criteria for assessment, scheme of evaluation and grading method.
- The Learning Process will be carried out through assessments of Knowledge, Skills and Attitude by various methods and the students will be given guidance to refer to the text books, reference books, journals, etc.

The faculty be able to –

Understand the principles of Learning

Understand the psychology of students

Develop instructional objectives for a given topic

Prepare course, unit and lesson plans

Understand different methods of teaching and learning

Use appropriate teaching and learning aids

Plan and deliver lectures effectively Provide feedback to students using various methods of Assessments and tools of Evaluation

Act as a guide, adviser, counselor, facilitator, and motivator and not just as a teacher alone

Signature of HOD Signature of faculty

Date: Date:

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Department of Electrical & Electronics Engineering

COURSE SCHEDULE

Academic Year : 2018-2019
Semester : II
Name of the Program: EEE…… B.Tech …II/II…..… Section: A,B

Course/Subject: ADE Lab…… Code: GR17A2046

Name of the Faculty: D.Karunakumar Dept: ……..EEE……

Designation: Assistant professor
The Schedule for the whole Course / Subject is:

Exp. No.	Description	Duration(Date)	Total No. of Periods
1.	Design of Operational Amplifier as proportional Amplifier	12-Dec	4
2.	Design of Operational Amplifier as integrator	19-Dec	4
3.	Design of Operational Amplifier as differential amplifier	26-Dec	4
4.	Design of Operational Amplifier as summation amplifier	02-Jan	4
5.	Design of Operational Amplifier for multiplying two time varying signals	09-Jan	4
6.	Design of Operational Amplifier for generation of triangle wave	16-Jan	4
7	Design of Operational Amplifier for generation of Square	23-Jan	4
8.	Design of Operational Amplifier for generation of sin wave	30-Jan	4
9.	555 timer as basic application of generating train of pulses	06-Feb	4
10	555 timer as speed sensor / frequency to Voltage Converter	13-Feb	4
11.	Design of Operational Amplifier as D/A converter	20-Feb	4
12.	Design of Operational Amplifier as V/f to F/v converter	27-Feb	4
13.	All gates using Xilinx software with Verilog code	06-Mar	4
14.	Internal Examination	13-Mar	4

Total No. of Instructional periods available for the course: …. …….Hours / Periods

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SCHEDULE OF INSTRUCTIONSCOURSEPLAN

Academic Year : 2018-2019

Semester : II

Name of the Program: EEE…… B.Tech …II/II…… Section: A,B

Course/Subject: ADE Lab…… Code:GR17A2046

Name of the Faculty: D.Karunakumar Dept: ……..EEE……
Designation: Assistant professor

Exp. No	Topics	Objectives & Outcomes	References(TextBook,Journal …)
1.	Design of Operational Amplifier as proportional Amplifier	1,2,3 & 1,2	M. Morris Mano and Michael D. Ciletti
2.	Design of Operational Amplifier as integrator	1,2,3 & 1,2	M. Morris Mano and Michael D. Ciletti
3	Design of Operational Amplifier as differential amplifier	1,2,3& 1,2	M. Morris Mano and Michael D. Ciletti
4	Design of Operational Amplifier as summation amplifier	1,2,3,6& 1,2	M. Morris Mano and Michael D. Ciletti
5	Design of Operational Amplifier for multiplying two time varying signals	1,2,3& 1,2	M. Morris Mano and Michael D. Ciletti
6	Design of Operational Amplifier for generation of triangle wave	1,2,3 & 1,2	M. Morris Mano and Michael D. Ciletti
7	Design of Operational Amplifier for generation of Square	1,2,3,4& 1,2	M. Morris Mano and Michael D. Ciletti
8	Design of Operational Amplifier for generation of sin wave	1,2,3 & 2	M. Morris Mano and Michael D. Ciletti

9	555 timer as basic application of generating train of pulses	1,2,3 & 2	M. Morris Mano and Michael D. Ciletti
10	555 timer as speed sensor / frequency to Voltage Converter	1,2,3& 2	M. Morris Mano and Michael D. Ciletti
11	Design of Operational Amplifier as D/A converter	1,2,3,& 2	M. Morris Mano and Michael D. Ciletti
12	Design of Operational Amplifier as V/f to F/v converter	1,2,3,4 ,5,6 & 2	M. Morris Mano and Michael D. Ciletti

Signature of HOD

Date:

Signature of faculty

Date:

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

COURSE OUTCOME AND PROGRAM OUTCOME MAPPING

PO's / CO's	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	H	H	H	M		H		M	H	H	H	H
CO2		H	H	M		H			M	H	H	H
CO3	H	M		H		M	H		M			M
CO4	H		H	M		M	H	M	M		H	M
CO5	H	H	M	M		H	H	H			H	M
CO6		H	H	M		H	H	M	H	M	H	H
CO7	H	H	H	M		H		M	H		H	H

Assessment methods:

1. Operation skill and familiarization ofsoftware.
2. Experimental procedure, simulation results, internal observation, labrecord.
3. Internal examinations.
4. External examinations.
5. Viva-voce.

1. **Course Objectives-Program Outcomes (POs) Relationship Matrix** (Indicate the relationships by mark "X")

P-Outcomes / C-Objectives	A	B	c	d	e	F	g	h	i	j	k	l
1	X	X	X	X	X				X	X	X	X
2	X				X		X	X		X	X	
3	X	X	X			X	X	X	X		X	X
4				X	X	X		X	X	X	X	
5		X	X	X					X	X		
6				X	X	X		X		X	X	
7	X	X	X	X	X	X	X		X	X	X	

2. **Course Outcomes-Program Outcomes (POs) Relationship Matrix** (Indicate the relationships by mark"X")

P-Outcomes / C-Outcomes	a	b	c	d	e	f	g	h	i	J	K	l
1	X	X	X	X	X			X	X	X	X	X
2	X	X	X	X	X	X	X	X	X	X	X	X
3	X	X	X	X	X	X	X	X	X	X	X	X
4	X	X	X							X	X	X
5	X	X	X							X	X	X
6	X	X	X							X	X	X
7	X	X	X							X	X	X

3. **Courses (with title & code)-Program Outcomes (POs) Relationship Matrix** (Indicate the relationships by mark "X"

P-Outcomes / Courses	a	b	c	d	e	f	g	h	i	j	K	l
Electrical Networks Lab	X	X	X	X	X	X	X	X	X	X	X	X

4. **Program Educational Objectives (PEOs) –Vision/Mission Matrix** (Indicate therelationships by mark "X")

PEOs	**Mission of department**			
	Higher Learning	Contemporary Education	Technical knowledge	Research
Graduates will have a successful technical or professional careers, including supportive and leadership roles on multidisciplinary teams	X	X	X	X
Graduates will be able to acquire, use and develop skills as required for effective professional practices		X	X	
Graduates will be able to attain holistic education that is an essential prerequisite for being a responsible member of society	X		X	
Graduates will be engaged in life-long learning, to remain abreast in their profession and be leaders in our technologically vibrant society.	X		X	X

5. **Program Educational Objectives(PEOs)-Program Outcomes(POs) Relationship Matrix** (Indicate the relationships by m

P-Outcomes / PEOs	a	b	c	d	e	f
1	X	X	X	X	X	

2	X	X	X	X	X	
3		X	X	X		X
4				X		

6.**Course Objectives-Course Outcomes Relationship Matrix** (Indicate the relationships by mark "X")

Course-Outcomes / Course-Objectives	1	2	3	4	5	6	7
1	X	X	X	X	X	X	X
2	X	X	X	X	X	X	X
3	X	X					
4				X	X		
5			X	X	X	X	X
6			X	X	X	X	X
7	X		X	X	X	X	

Program Educational Objectives (PEOs)-Course Outcomes Relationship Matrix (Indicate the relationships by mark

P-Objectives(PEO) / Course-Outcomes	1	2	3	4
1	X	X		X
2	X	X		X
3	X	X		X
4	X	X		X
5	X	X		X
6	X	X		X
7	X	X		X

8. Assignments & Assessments-Program Outcomes (POs) Relationship Matrix (Indicate the relationships by mark "X"

P-Outcomes / Assessments	A	b	c	d	e	f
1	X	x		x		x
2	X	x	x			x

3	X	x	x			x
4	X	x	x			x

9. Assignments & Assessments-Program Educational Objectives (PEOs) Relationship Matrix (Indicate the relationships by

P-Objectives (PEOs) Assessments	1	2	3	4
1	X	X		
2		X		
3		X	X	X
4		X		
5		X		

Assessment process and Relevant Surveys conducted:

1. Constituencies -Program Outcomes (POs) Relationship Matrix (Indicate the relationships by mark "X").

Constituencies

1. **Alumni**
2. **Governmentemployers**
3. **Students**

P-Outcomes / Constituencies	a	b	c	d	e	f	G	h	i	j	k	l
1	X	X	X	X	X	X	X		X	X		X
2	X	X	X	X	X	X	X		X			X
3	X	X			X	X	X	X		X	X	X

9	CO-Cognitive Level Mapping

Subject :ADE Lab

CO	Cognitive Learning Level					
	1	2	3	4	5	6
1		X				
2			X			
3						X
4				X		

5		X				
6			X			
7		X				

Cognitive Learning Levels:

CLL1: Remembering

CLL2: Understanding

CLL3: Applying

CLL4: Analyzing

CLL5: Evaluating

CLL6: Creating

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

EVALUATION STRATEGY

Academic Year : 2018-2019

Semester : II

Name of the Program: EEE…… B.Tech …II/II…..… Section: A,B

Course/Subject: ADE Lab…… Code: GR17A2046

Name of the Faculty: D.Karunakumar Dept: ……..EEE……

Designation: Assistant professor

1. TARGET:

A) Percentage for pass: 100%

2. COURSE PLAN & CONTENT DELIVERY

- PPT presentation of the Lectures
- Solving exercise problems
- Model questions

3. METHOD OF EVALUATION

3.1 ☐ Daily Attendance

3.2 ☐ Lab records and observation

3.3 ☐ Mini Projects

3.4 ☐ Viva Voce

3.5 ☐ Internal Examination

3.6 ☐ Semester/End Examination

4. List out any new topic(s) or any innovation you would like to introduce in teaching the subjects in this Semester.

Signature of HOD Signature of faculty

Date: Date:

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RUBRIC

OBJECTIVE: **Work effectively with others**

STUDENT OUTCOME: **Ability to function in a multi-disciplinary team**

S.No.	Student Name	Performance Criteria	Unsatisfactory	Developing	Satisfactory	Exemplary	Score
			1	2	3	4	
1.	R.Madhuri (18245A0218)	**Research & Gather Information**	Does not collect any information that relates to the topic.	Collects very little information some relates to the topic	Collects some basic Information most relates to the topic.	Collects a great deal of Information all relates to the topic.	
		Fulfill team role's	Does not perform any duties of assigned team role.	Performs very little duties.	Performs nearly all duties.	Performs all duties ofassigned team role.	
		Share Equally	Always relies on others to do the work.	Rarely does the assigned work--often needs reminding.	Usually does the assigned work--rarely needs reminding.	Always does the assigned work without having to be reminded	

		Listen to other team mates	Is always talking--never allows anyone else to speak.	Usually doing most of the talking--rarely allows others to speak.	Listens, but sometimes talks too much.	Listens and speaks a fair amount.	
						Average score	
2.	Revanth (17241A02B0)	**Research & Gather Information**	Does not collect any information that relates to the topic.	Collects very little information --some relates to the topic	Collects some basic informatio n--most relates to the topic.	Collects a great deal of informati on--all relates to the topic.	
		Fulfill team role's	Does not perform any duties of assigned team role.	Performs very little duties.	Performs nearly all duties.	Performs all duties of assigned team role.	
		Share Equally	Always relies on others to do the work.	Rarely does the assigned work--often needs reminding.	Usually does the assigned work--rarely needs	Always does the assigned work without having to	

					reminding.	be reminded .	
		Listen to other team mates	Is always talking--never allows anyone else to speak.	Usually doing most of the talking--rarely allows others to speak.	Listens, but sometimes talks too much.	Listens and speaks a fair amount.	
						Average score	
3	R.V.Sai Tarun (17241A02A4)	**Research & Gather Information**	Does not collect any information that relates to the topic.	Collects very little information --some relates to the topic	Collects some basic informatio n--most relates to the topic.	Collects a great deal of informati on--all relates to the topic.	
		Fulfill team role's	Does not perform any duties of assigned team role.	Performs very little duties.	Performs nearly all duties.	Performs all duties of assigned team role.	
		Share Equally	Always relies on others to do	Rarely does the assigned	Usually does the assigned	Always does the assigned	

			the work.	work--often needs reminding.	work--rarely needs reminding.	work without having to be reminded	
		Listen to other team mates	Is always talking--never allows anyone else to speak.	Usually doing most of the talking--rarely allows others to speak.	Listens, but sometimes talks too much.	Listens and speaks a fair amount.	
						Average score	

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INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electrical & Electronics Engineering

COURSE COMPLETION STATUS

Academic Year : 2018-2019

Semester : II

Name of the Program: EEE…… B.Tech …II/II…..… Section: A,B

Course/Subject: ADE Lab…… Code: GR17A2046

Name of the Faculty: D.Karunakumar Dept: ……..EEE……

Designation: Assistant professor

Program	Remarks	No. of Objectives Achieved	No. of Outcomes Achieved
1	1 & 2 programs completed by 18/12/18		
2		2,3, 4	2,4
3	3 & 4 programs completed by 22/12/18		
4		1,3	2,4
5	5 program completed by 26/01/19	1,3	2,4
6	6 program completed by 29/01/19	1,3	2,4
7	7 program completed by 02/02/19	1,3	2,4
8	8 program completed by 16/02/19	1,3	2,4
9	9 program completed by 23/02/19	1,3	2,4
10	10 program completed by 30/02/19	1,3	2,4
11	11 & 12 program completed by 06/03/19	1,2	2,3
12		1,3	2,1,5
13	13 program completed by 13/03/19	1,3	2,1,5
14	14 programs completed by 27/03/19	1,3	2,1,5
15	15 programs completed by 01/04/19	2,3	1,2,3,6 ,7

Signature of HOD Signature of faculty

Date: Date:

Note: After the completion of each unit mention the number of Objectives & Outcomes Achieved.

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Department of Electrical & Electronics Engineering

GUIDELINES TO STUDY THE COURSE/SUBJECT

Academic Year : 2018-2019

Semester : II

Name of the Program: EEE…… B.Tech …II/II…… Section: A,B

Course/Subject: ADE Lab…… Code: GR17A2046

Name of the Faculty: D.Karunakumar Dept: ……..EEE……

Designation: Assistant professor

Course Design and Delivery System (CDD):

- The Course syllabus is written into number of learning objectives and outcomes.
- These learning objectives and outcomes will be achieved through lectures, assessments, assignments, experiments in the laboratory, projects, seminars, presentations, etc.
- Every student will be given an assessment plan, criteria for assessment, scheme of evaluation and grading method.
- The Learning Process will be carried out through assessments of Knowledge, Skills and Attitude by various methods and the students will be given guidance to refer to the text books, reference books, journals, etc.

The faculty be able to –

- Understand the principles of Learning
- Understand the psychology of students
- Develop instructional objectives for a given topic
- Prepare course, unit and lesson plans
- Understand different methods of teaching and learning
- Use appropriate teaching and learning aids
- Plan and deliver lectures effectively
- Provide feedback to students using various methods of Assessments and tools of Evaluation
- Act as a guide, advisor, counselor, facilitator, motivator and not just as a teacher alone

Signature of HOD
Date:

Signature of faculty
Date: